High Speed Read operation by using DDR3 SDRAM Controller

Shaik Riyazuddien
Department of ECE
Vasireddy Venkatadri Institute of Technology, Nambur, India

Sarada Musala
Department of ECE
Vignan University, Vadlamudi, India,

Mariyadasu Ammuluri
Department of ECE
VLITS, Vadlamudi, India

Abstract— ***In computing, DDR3 SDRAM or double-data- rate three synchronous dynamic random access memories is a random access memory interface technology used for high bandwidth storage of the working data of a computer or other digital electronic devices. DDR3 SDRAM is the 3rd generation of DDR memories, featuring higher performance and lower power consumption. In comparison with earlier generations, DDR1/2 SDRAM, DDR3 SDRAM is a higher density device and achieves higher bandwidth due to the further increase of the clock rate and reduction in power consumption.***

In this work, the DDR3 SDRAM controller is designed and it can interface with Look up table based Hash CAM circuit. Content-addressable memory (CAM) is a special type of computer memory used in certain very high speed searching applications. Because a CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all search applications. The architecture of DDR3SDRAM controller consists of Initialization FSM, Command FSM, data path, bank control, clock counter, refresh counter, Address FIFO, command FIFO, Wdata FIFO and Rdata reg.

Now here an advanced DDR3 SDRAM controller architecture was designed and which can interface with a high performance Hash-CAM based lookup circuit. Basically the DDR3 SDRAM controller can perform normal write, normal read and fast write operations, in this paper a ddr3 controller is designed to achieve fast read operation to achieve high performance throughput in many network systems and these results are verified by simulation and DDR3 SDRAM controller is synthesized.

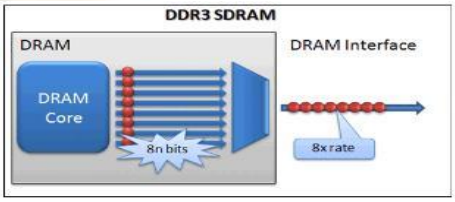
Keywords—DDR3; SDRAM; FIFO; Wdata; Rdata

I. INTRODUCTION

In the recent advanced developed network systems, the processing techniques of data, i.e. in packets form which deal with massive content to achieve high throughput packet of the internet. Now a day's according to the advances in memory architecture we must need to meet the bandwidth requirements. Content based techniques are widely used for achieving fast table lookup. Unlike standard computer memory (random access memory or RAM) in which the user supplies a memory address and the RAM returns the data word stored at that address, a CAM is designed such that the user supplies a data word and the CAM searches its entire memory to see if that data word is stored anywhere in it. If the data word is found, the CAM returns a list of one or more storage address where the word was found (and in some architecture, it also returns the data word, or other associated pieces of data). Recently a Hash-CAM circuit, which combines the advantages of hash algorithm and CAM functionality was used in the place of pure CAM based lookup circuits with some comparable parameters like performance, higher memory density and lower cost. Here the efficient bandwidth usage is major part for lookup functions. However, a DDR3 SDRAM controller must be designed to achieve good read efficiency and for high bandwidth.

II. DESIGN METHODOLOGY

DDR3 SDRAM devices are the next generation devices in the DDR SDRAM family. DDR3 SDRAM is third generation of DDR memories, providing higher performance and lower power consumption. The primary benefit of DDR3 is the ability to transfer I/O data at eight times the data rate of the memory cells it contains, thus enabling higher bus rates and higher peak rates than earlier memory technologies. However, there is no corresponding reduction in latency, which is therefore proportionally higher. In addition, the DDR3 standard allows for chip capacities of 512 megabits to 8 gigabits, effectively enabling a maximum memory module size of 16 gigabytes.



DDR3 SDRAM data rate

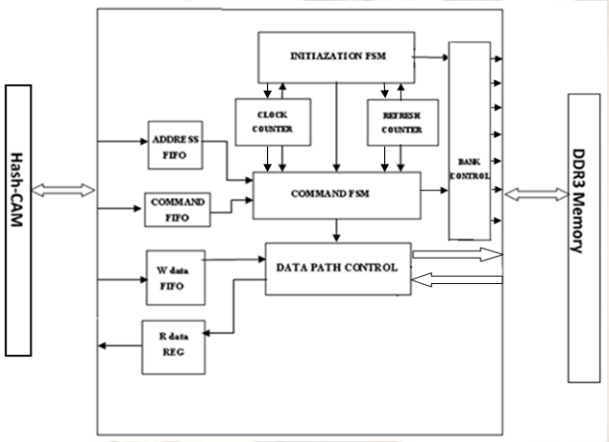
The frequencies of DDR3 memory could be raised beyond those of DDR2 due to doubling of the data prefetch that was moved from the information storage device to the input/output buffer. While DDR2 SDRAM uses 4-bit

samples, DDR3 SDRAM uses 8-bit prefetch also known as 8n-prefetch, as shown in fig 1. In other words, DDR3 SDRAM technology implies doubling of the internal bus width between the actual DRAM core and the input/output buffer. The proposed Hash-CAM based look up circuit is shown in Figure 2.

Hash-CAM lookup circuit for DDR3 SDRAM

The original data and reference address information are stored in the DDR3 SDRAM lookup request (data input) for a given content is pipelined and processed by the Hash circuit to generate an address. This address value is forwarded to DDR3 SDRAM Interface where it is translated into instructions and addresses that are recognized by the DDR3 memory as an access.

The stored data & addresses in the memory are read back to the Hash-CAM circuit in order to validate the match. In the case of corresponding reference address is reference address is returned.



Functional block diagram of DDR3 SDRAM Controller

The functional block diagram of the DDR3 controller is shown in Fig 3. The architecture of DDR3SDRAM controller consists of Initialization FSM Command FSM, data path, bank control, clock counter, refresh counter, Address FIFO, command FIFO, Wdata FIFO and Rdata reg.

Initialization FSM generates proper i_State to initialize the modules in the design. Command FSM generates c_State to perform the normal write, read and fast write, read operations. The data path module performs the data latching and dispatching of the data between Hash-CAM unit and DDR3SDRAM banks. The Address FIFO gives the address to the Command FSM so the bank control unit can open particular bank and address location in that bank. The Wdata FIFO provides the data to the data path module in normal and fast write operation. The Rdata reg gets the data from the data path module normal and fast read operation.

In this paper the designed DDR3 controller provides interface to the Hash-CAM circuit and the DDR Memory Banks. If the data word is found, the CAM returns a list of one or more storage addresses where the word was found (and in some architecture, it also returns the data word, or other associated pieces of data). Because a CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all search applications.

2.1 Timing and Bank Acess Control of DDR3 sdram

The most important parameters to consider in ddr3 technology are column address strobe latency (tCAS), RAS to CAS latency (tRCD), RAS precharge time (tRP), row active time (tRAS). The ddr3 commands are given below table 1. Depending on these commands only we can perform operations like auto refresh, write, read, precharge etc.

Step	Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
1	Load Mode	L	L	L
2	Auto Refresh	L	L	H
3	Precharge (1)	L	H	L
4	Bank Activate	L	H	H
5	Write	H	L	L
6	Read	H	L	H
7	No Operation/IDLE	H	H	H

DDR3 SDRAM commands

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Number equations consecutively. Equation numbers, within parentheses, are to position flush right, as in (1), using a right tab stop. To make your equations more compact, you may use the solidus (/), the exp function, or appropriate exponents. Italicize Roman symbols for quantities and variables, but not Greek symbols. Use a long dash rather than a hyphen for a minus sign. Punctuate equations with commas or periods when they are part of a sentence, as in

$$a + b = \gamma$$

Note that the equation is centered using a center tab stop. Be sure that the symbols in your equation have been defined before or immediately following the equation. Use "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ..."

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- The word "data" is plural, not singular.
- The subscript for the permeability of vacuum μ_0, and other common scientific constants, is zero with subscript formatting, not a lowercase letter "o."
- In American English, commas, semi-/colons, periods, question and exclamation marks are located within quotation marks only when a complete thought or name is cited, such as a title or full quotation. When quotation marks are used, instead of a bold or italic typeface, to highlight a word or phrase, punctuation should appear outside of the quotation marks. A parenthetical phrase or statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.)
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An excellent style manual for science writers is [7].

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After the text edit has been completed, the paper is ready for the template. Duplicate the template file by using the Save As command, and use the naming convention prescribed by your conference for the name of your paper. In this newly created file, highlight all of the contents and import your prepared text file. You are now ready to style your paper; use the scroll down window on the left of the MS Word Formatting toolbar.

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TABLE I. TABLE STYLES

Table Head	**Table Column Head**		
	Table column subhead	***Subhead***	***Subhead***
copy	More table copy[a]		

[a.] Sample of a Table footnote. *(Table footnote)*

Fig. 1. Example of a figure caption. *(figure caption)*

Figure Labels: Use 8 point Times New Roman for Figure labels. Use words rather than symbols or abbreviations when writing Figure axis labels to avoid confusing the reader. As an example, write the quantity "Magnetization," or "Magnetization, M," not just "M." If including units in the label, present them within parentheses. Do not label axes only with units. In the example, write "Magnetization (A/m)" or "Magnetization (A (m(1)," not just "A/m." Do not label axes with a ratio of quantities and units. For example, write "Temperature (K)," not "Temperature/K."

ACKNOWLEDGMENT *(Heading 5)*

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[1] G. Eason, B. Noble, and I.N. Sneddon, "On certain integrals of Lipschitz-Hankel type involving products of Bessel functions," Phil. Trans. Roy. Soc. London, vol. A247, pp. 529-551, April 1955. (*references*)
[2] J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.
[3] I.S. Jacobs and C.P. Bean, "Fine particles, thin films and exchange anisotropy," in Magnetism, vol. III, G.T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271-350.
[4] K. Elissa, "Title of paper if known," unpublished.
[5] R. Nicole, "Title of paper with only first word capitalized," J. Name Stand. Abbrev., in press.
[6] Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interface," IEEE Transl. J. Magn. Japan, vol. 2, pp. 740-741, August 1987 [Digests 9th Annual Conf. Magnetics Japan, p. 301, 1982].
[7] M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.

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